> "Where a reference is relied on to support a rejection, whether or not in a minor capacity, that reference should be positively included in the statement of the rejection."

In the final office action, the Examiner for the first time communicates the basis for the rejection of claim 10. By making the office action final, the Examiner deprives the applicant of a fair opportunity to reply, contrary to the requirements of MPEP § 706.02(j). Moreover, the Examiner for the first time cites a new reference (the USB 1.0 specification) and communicates the basis for reliance on the contents of that reference, but without positively including the reference in the rejection, contrary to the requirements of MPEP § 706.02(j).

The Examiner disingenuously sets forth new grounds of rejection and new bases for rejections in the Response to Arguments on pages 2 through 4 of the final office action. With all due respect, this type of gamesmanship unnecessarily protracts the prosecution of the application. Applicants note that the Examiner's Response to Arguments does not form any part of the rejections.

Claims 1-6, 10-11, and 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 5,081,654 (Stephenson) in view of U.S. Pat. No. 6,707,396 (Govindaraman). Applicants respectfully traverse this rejection for the following reasons.

With respect to claim 1, the rejection of record states that "Govindaraman teaches the use of a NRZI decoder module to decode received USB NRZI data using parallel processing." See final office action, page 5, lines 3-4. The Examiner has now admitted that this is incorrect: "In regards to applicants arguments that Govindaraman teaches the sync detect being in a serial stream: The examiner agrees." See final office action, page 2, lines 15-16. As previously noted by the applicants, the NRZI decoder 240 is likewise in the serial stream. Accordingly, the Examiner has admitted that the rejection of record

is in error because the NRZI decoder 240 of Govindaraman does not use parallel processing.

Applicants do not understand why the Examiner did not withdraw the rejection, or at least re-state or re-formulate the rejection. But as it stands, the rejection of record is admittedly erroneous and should be withdrawn.

Moreover, with respect to claim 1, the rejection is internally inconsistent. The rejection identifies Stephenson as the primary reference and alleges that Stephenson teaches various claim recitations including (paraphrasing from the final office action):

- an integrated circuit;
- a parallel frame delineation module (20);
- a plurality of concurrent comparators (32, 34);
- to delineate received frame boundaries (abstract);
- within a data stream (22).

The rejection then admits that Stephenson (the primary reference) lacks the NRZI decoder module to decode received USB NRZI using parallel data processing and appears to rely on Govindaraman (the secondary reference) to provide the missing teaching (now admitted to be erroneous). However, the rejection then proposes to modify the secondary reference (Govindaraman) with some unidentified sync detect from the primary reference (Stephenson). The proposed modification is internally inconsistent with the remainder of the rejection and fails to establish how Govindaraman, after the proposed modification, would teach or suggest all of the claim recitations (which are otherwise alleged to be contained in Stephenson, not in Govindaraman).

Applicants requested clarification of the Examiner's position and in the Examiner's Response to Arguments the Examiner cites the title, the abstract, every figure, and every column of Stephenson. See final office action at page 2, lines 8-10. Applicants fail to understand how this clarifies the Examiner's position or advances the prosecution.

Applicants do not understand why the Examiner did not withdraw the rejection, or at least re-state or re-formulate the rejection. But as it stands, the rejection of record is erroneous and should be withdrawn.

In any event, the rejection of record fails to establish even a prima facie case of obviousness. Claim 1 recites, among other things, an NRZI decoder module to decode received NRZI encoded data using parallel data processing. The final office action admits that "Stephenson does not teach the ... NRZI decoder using parallel processing." See final office action at page 5, lines 1-3. The Examiner now agrees that the components along data path 110 in Govindaraman are serial components (at least until the serial to parallel converter 260), including the sync detect 230, the NRZI decoder 240, and the bit un-stuffer 250. Accordingly, Govindaraman also fails to teach or suggest the recited NRZI decoder module to decode received NRZI encoded data using parallel data processing. Because neither reference teaches or suggests, among other things, the recited NRZI decoder module to decode received NRZI encoded data using parallel data processing, the rejection of record fails to establish a prima facie case of obviousness and no combination of the references can possibly teach or suggest all of the claim recitations of claim 1.

Applicants note that applicants are not arguing the references individually, but rather are arguing that any proposed combination still fails to establish a prima facie case of obviousness. Assuming for the sake of argument, that the sync detect 230 of Govindaraman was replaced with some as yet unidentified sync detect from Stephenson, the resulting circuit would still lack the recited NRZI decoder module to decode received NRZI encoded data using parallel data processing.

Finally, with respect to claim 1, the Examiner provides only a contrived motivation to modify Govindaraman with the teachings of Stephenson, namely "because this would have for the handling of high speed data streams in parallel." In fact, Govindaraman handles high speed data streams already ("for example, 480 Mbit/sec used in USB 2.0 devices", see col. 2, lines 59-60). Moreover, Govindaraman teaches that the

sync detector 230 operates at a lower local clock rate for parallel processing. See Govindaraman, col. 2, lines 55-62. No one of ordinary skill in the art would find it necessary or desirable to modify the state of the art circuit disclosed in Govindaraman (which can already handle "high speed data streams" in serial and/or parallel) with the fifteen year old technology described in Stephenson.

To the extent that the Examiner may be suggesting that Govindaraman be modified to use the parallel frame synchronization circuit 20 of Stephenson instead of the sync detect circuit 230, the combination is unworkable and has no reasonable expectation of success. Applicant note that the circuit 20 includes a serial to parallel converter 24 so that, in the proposed modification, data provided to the admittedly serial NRZI decoder 240, serial bit un-stuffer 250, and later serial to parallel converter 260 would be indecipherable. It is clear that substantially further modification to the circuit 100 would be required to arrive at any type of workable system. In any event, neither of the references teaches or suggests anything whatsoever that would enable one of ordinary skill in the art to construct a parallel NRZI decoder or a parallel bit un-stuffer.

Because the rejection of record in the final office action is facially erroneous and logically inconsistent, and because the office action fails to establish a prima facie case of obviousness, and because the proposed motivation to combine the references is erroneous, and because the proposed modification is unworkable, claim 1 is patentable over any combination of Stephenson and Govindaraman. Claims 2-6 depend either directly or indirectly from claim 1 and are likewise patentable.

With respect to claim 5, applicants provide the following side-by-side comparison for the Examiner's convenience:

Claim 5:	Rejection of claim 5:	Column 1 lines 20-26
5. The integrated circuit of claim 3, wherein the parallel frame boundary delineation module further comprises a parallel start-of-packet detector.	In regards to claim 5: Stephenson teaches detecting the start of frame by matching a framing pattern (Column 1 lines 20-26).	Generally frame synchronization of an incoming serial bit data stream is performed by comparing a known framing pattern to the incoming data which contains periodic frame synchronization information so as to determine the frame boundary (start of frame) based upon matching the frame synchronization information to the framing pattern.

The rejection of claim 5 is not understood because the language cited in the office action does not correspond to the claim language and the cited portion of the reference does not appear to read on the claim language. Clarification was respectfully requested, but no clarification was provided. Applicants respectfully remind the Examiner of the requirements of MPEP § 707.07(f):

707.07(f) Answer All Material Traversed [R-1]

>In order to provide a complete application file history and to enhance the clarity of the prosecution history record, an examiner must provide clear explanations of all actions taken by the examiner during prosecution of an application.<

Where the requirements are traversed, or suspension thereof requested, the examiner should make proper reference thereto in his or her action on the amendment.

Where the applicant traverses any rejection, the examiner should, if he or she repeats the rejection, take note of the applicant's argument and answer the substance of it.

The Examiner has yet to communicate any proper basis for the rejection of claim 5. By making the office action final, the Examiner deprives the applicant of a fair opportunity to reply, contrary to the requirements of MPEP § 706.02(j).

Applicants do not know if the rejection is simply a typographical or editorial error, or if the Examiner is actually asserting that the cited portion of col. 1, lines 20-26

reads on claim 5. Applicants notes that the cited portion appears to relate only to serial operations, and not to any parallel start-of-packet detector. Applicants cannot further respond to a rejection of claim 5 which has not been clearly explained by the Examiner, contrary to the requirements of MPEP § 706.02(j) and MPEP § 707.07(f), other than to note that by failing to identify how the cited portion reads on the claim recitations the Examiner has failed to establish a prima facie case of obviousness.

With respect to claim 10, the rejection of record completely fails to address the recitations of claim 10. Claim 10 is a method claim having a different scope as compared to claim 1. For example, the office completely fails to mention any recitations of claim 10 including at least: asserting a flag upon detection of the frame delineation marker; and creating a vector indicating a location of a frame boundary in the data stream. Applicants submit that neither of the cited references, alone or in combination, teach or suggest asserting a flag upon detection of the frame delineation marker; and creating a vector indicating a location of a frame boundary in the data stream. Accordingly, claim 10 and its dependent claims 11-16 are believed to be patentable.

In the Examiner's Response to Arguments, the Examiner asserts that the office action addresses the recitations of claim 10 on page 2. Claim 10 recites, among other things:

> searching for a frame delineation marker in the data received using concurrent comparators;
>
> asserting a flag upon detection of the frame delineation marker; and
>
> creating a vector indicating a location of a frame boundary in the data stream.

Applicants have thoroughly reviewed page 2 of the prior office action and cannot find any of the following terms from the foregoing recitations: searching, marker, asserting, flag, creating, vector, indicating, or location. The rejection of record is sorely deficient and should be withdrawn.

Applicants further note that the Examiner's comments in the Response to Arguments form no part of the rejection of record. Assuming, for the sake of argument, that the Board would give any weight to such comments, applicants note that the comments fall far short of meeting the requirements under MPEP § 706.02(j) for the contents of a 35 U.S.C. § 103 rejection.

In order to expedite the prosecution, applicants further note that the terms 'flag' and 'vector' cannot be located anywhere in either the Stephenson or the Govindaraman references. Applicants further note that the output signal 42 is not a flag and does not appear to asserted upon detection of any frame delineation marker. Applicants further note that 'F6' and '28' are not vectors and, if they were, they are not vectors indicating the location of the frame boundary in the data stream (they are at most markers in the data stream).

Because the rejection of record fails to identify how the recitations of claim 10 are allegedly taught or suggested by the references, the Examiner has failed to establish a prima facie case of obviousness and claim 10 is patentable over the cited references.

With respect to claim 16, the claim recites that the vector created comprises an eleven-bit vector. Applicants maintain that the relied upon 16 output bits of comparators 32 and 34 do not relate to the recited eleven-bit vector. In fact, the output of comparators 32 and 34 do not relate to any vector indicating a location of a frame boundary in the data stream.

Claims 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stephenson in view of U.S. Pat. No. 5,884,086 (Amoni). Applicants respectfully traverse this rejection for the following reasons.

Claim 7 recites one or more Universal Serial Bus (USB) connectors to couple to a communications channel carrying a USB data stream; an application specific integrated circuit comprising a USB transceiver, a serial interface engine and apparatus-specific logic, the USB transceiver having concurrent comparators to delineate received asynchronous frame boundaries within the USB data stream and parallel logic to decode received encoded data. The rejection of record asserts, without support or citation to any

text portion or drawings element, that Amoni discloses a USB transceiver, a serial interface engine, and apparatus specific logic. In fact, Amoni makes no reference to such elements. Accordingly, the rejection of record fails to establish a prima facie case of obviousness. Amoni is related to providing power to USB 1.0 peripherals and does not discuss the transceiver / serial interface aspects of the USB devices.

In any event, the rejection of record provides only a contrived motivation to combine the references. The rejection of record proposes to modify Amoni with the teachings of Stephenson 'because this would have for the handling of high speed data streams in parallel." Amoni, as noted above, is concerned with power delivery to USB 1.0 devices, and has no need for handling high speed data streams in parallel. As explicitly stated several times in Amoni, the top supported speed is 12 Mbits. In fact, Stephenson teaches away from the combination. Stephenson clearly states that the circuit disclosed therein is useful for data streams above 50 MHz (see col. 1, lines 27-34, col. 2, lines 32-40, and col. 5, line 66 - col. 6, line 3). Absent the hindsight afforded by the present specification, one of ordinary skill in the art would not be motivated to modify Amoni with the circuit of Stephenson because Stephenson's circuit is simply not necessary for handling a 12 Mbit data stream.

In any event, the rejection of record fails to establish even a prima facie case of obviousness. Claim 7 recites, among other things, parallel logic to decode received encoded data. The office action admits in connection with claim 1 that Stephenson fails to teach NRZI decoding. In fact, Stephenson does not teach anything whatsoever with respect to decoding encoded data, parallel or otherwise. The data stream in Stephenson is simply not encoded. The rejection of record does not cite any portion of Amoni for this missing teaching.

Applicants note that applicants are not arguing the references individually, but rather are arguing that any proposed combination still fails to establish a prima facie case of obviousness. Assuming for the sake of argument, that Amoni was somehow modified to use the start of frame detect from Stephenson, the resulting circuit would still lack the recited parallel logic to decode received encoded data.

Because the rejection of record fails to establish a prima facie case of obviousness and because the proposed motivation to combine the references is erroneous, claim 7 is patentable over Stephenson in view of Amoni. Dependent claims 8 and 9 are likewise patentable.

Applicants note that claim 9 further recites that the parallel logic decodes non-return to zero invert (NRZI) encoded data, which was admitted as being absent from the techings of Stephenson. Although Amoni mentions NRZI, Amoni does not teach or suggest parallel logic to decode NRZI encoded data.

The Examiner disingenuously attempts to cure some of the above deficiencies by making new grounds of rejection in the Examiner's Response to Arguments. Applicants note that the Examiner's comments in the Response to Arguments form no part of the rejection of record. In several instances the Examiner relies on citations to a newly cited reference which is not of record in the rejection. By doing so, the Examiner has implicitly admitted that the rejection of record is deficient. Applicants do not understand why the Examiner did not withdraw the rejection, or at least re-state or re-formulate the rejection. But as it stands, the rejection of record is admittedly erroneous and should be withdrawn.

In order to expedite the prosecution of the application, applicants further note that none of the cited references, namely Stephenson, Amoni, or the USB 1.0 Spec, teach or suggest the recited parallel logic to decode received encoded data.

Claims 12-13 and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stephenson in view of Govindaraman and further in view of U.S. Pat. No. 6,041,430 (Yamauchi). Applicants respectfully traverse this rejection for the following reasons.

With respect to claims 12-13, these claims depend either directly or indirectly from patentable claim 10, and are also believed to be patentable. Yamauchi, which is

relied upon for elements of claims 12 and 13, fails to make up for the deficiencies in the other references with respect to claim 10.

With respect to claim 17, for at least the reasons given above with respect to claim 1, the office action fails to establish motivation to combine Stephenson and Govindaraman, and further because the proposed modification is unworkable, claim 17 is patentable over the combination of Stephenson and Govindaraman. Claims 18-19 depend either directly or indirectly from claim 17 and are likewise patentable.

In view of the foregoing, favorable reconsideration and withdrawal of the rejections is respectfully requested. Early notification of the same is earnestly solicited. If there are any questions regarding the present application, the Examiner is invited to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

January 28, 2005
Date

Paul E. Steiner
Reg. No. 41,326
(703) 633 - 6830

Intel Americas
LF3
4030 Lafayette Center Drive
Chantilly, VA 20151

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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